What is claimed is:

1. An output driver in a semiconductor memory device including a plurality of blocks of memory cells, wherein a first of the blocks transmits data to a data input/output line through the output driver, the output driver comprising:

a first transistor connected to a reference voltage, the first transistor being responsive to the data from the first block;

a second transistor between the first transistor and the data input/output line; and

a controller coupled to control the second transistor, the controller being operable in a first mode in which the second transistor is responsive to a column cycle signal for selecting the first block, wherein the data from the first block is transmitted to the data input/output line via the first and second transistors when the second transistor responds to the column cycle signal.

2. The output driver of claim 1, wherein the controller deactivates the second transistor when a second of the blocks is selected for data output.

3. The output driver of claim 1, wherein the controller activates the second transistor when the second transistor responds to the read control signal, and the data from the first block is transmitted to the data input/output line via the first and second transistors.

4. The output driver of claim 1, wherein the control is further operable in a second mode in which the second transistor is responsive to a read control signal containing calibration information about characteristics of the data input/output line.

5. The output driver of claim 4, wherein the controller comprises a multiplexer that selectively transmits one of the column cycle signal and the read control signal to the gate of the second transistor in response to a clock enable signal.

6. The output driver of claim 4, wherein the characteristics of the data input/output line comprise an output current (I_{OL}) characteristic for adjusting a signal level of the data input/output line and a temperature characteristic (TMIN/MAX) for adjusting a slew rate of the output driver according to change in temperature.

7. A memory module comprising:

a plurality of semiconductor memory devices, each semiconductor memory device including a plurality of blocks of memory cells and a plurality of output drivers corresponding to the blocks, the blocks transmitting data through output drivers;

channel bus lines shared by the data input/output lines, wherein:

in one semiconductor memory device, the data of a selected block is transmitted to one of the channel bus lines via a corresponding output driver, which is activated in response to a column cycle signal selecting the block, and via one of the data input/output line, while in the remaining semiconductor memory devices sharing the channel bus line, the output drivers are all deactivated, and wherein

each output driver comprises:

a first transistor connected to a reference voltage, the first transistor responsive to the memory cell data; and

a second transistor for selectively connecting the first transistor to the data input/output line in response to the column cycle signal or a read control signal containing calibration information about characteristics of the data input/output line.

8. The memory module of claim 7, wherein the second transistors of output drivers in the blocks are simultaneously activated when the second transistors respond to the read control signal, and the memory cell data of the selected block is transmitted to the data input/output line via the first and second transistors.

9. The memory module of claim 7, further comprising a multiplexer for selectively transmitting one of the column cycle signal and the read control signal to the gate of the second transistor in response to a clock enable signal.

10. The memory module of claim 7, wherein the characteristics of the data input/output line are an output current (I_{OL}) characteristic of adjusting the signal level of the data input/output line and a temperature characteristic (TMIN/MAX) of adjusting the slew rate of the output driver according to change in temperature.

11. A semiconductor memory device comprising:

a plurality of output drivers; and

a plurality of blocks of memory cells corresponding to and respectively coupled to the

plurality of output drivers, wherein each block transmits data to through the corresponding output driver, wherein

each output driver comprises:

a first transistor connected to a reference voltage, the first transistor being responsive to the data from the corresponding block;

a second transistor connected to the first transistor; and

a controller connected to control the second transistor, the controller being operable in a first mode in which the second transistor is responsive to a column cycle signal for selecting the block corresponding to the output driver and operable in a second mode in which the second transistor is responsive to a read control signal containing calibration information about characteristics of a data input/output line connected to the second transistor, wherein the data from the corresponding block is transmitted to the data input/output line via the first and second transistors when the second transistor responds to the column cycle signal.

12. The semiconductor memory device of claim 11, wherein the controllers deactivate the second transistors of the output drivers in unselected blocks.

13. The semiconductor memory device of claim 11, wherein:

the controllers activate simultaneously the second transistors of output drivers when the second transistors respond to the read control signal; and

each controller separately activates the associated second transistor when cell data of the selected DQ block is transmitted to the data input/output line via the first and second transistors.

14. The semiconductor memory device of claim 11, each controller comprising a multiplexer that selectively transmits one of the column cycle signal and the read control signal to the gate of the second transistor in response to a clock enable signal.

15. The semiconductor memory device of claim 11, wherein the characteristics of the data input/output line comprise an output current (I_{OL}) characteristic for adjusting a signal level of the data input/output line and a temperature characteristic (TMIN/MAX) for adjusting a slew rate of the output driver according to change in temperature.